A Compact Full MMIC Module for *Ku*-Band Phase-Locked Oscillators

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Abstract—**A compact *Ku*-band phase-locked oscillator module has been developed in a full MMIC configuration. The module includes an MMIC voltage-controlled oscillator, an analog frequency divider, and interstage amplifiers. The constituent monolithic chips are integrated in a very small single-package module and operate at the target frequencies without any external trimming or matching network. The oscillator is tuned more than 1 GHz with a constant output amplitude. The frequency-divided output is also obtained over the whole tuning range. Spurious output is not found at any frequency up to 22 GHz. In spite of the very low Q factor of GaAs monolithic circuitry, the oscillator phase noise exhibited is less than −80 dBc/Hz, due to the high-gain, high-speed phase lock.**

I. Introduction

MONOLITHIC microwave integrated circuits (MMIC's) have great potential in reducing the size of microwave equipment. Several kinds of amplifiers and mixers have been developed and some of them have already been put into practical use for lower microwave frequencies. However, with regard to microwave oscillators, MMIC implementation has not yet been reported for practical systems. In attempts to introduce MMIC's into oscillator systems, some MMIC's have been fabricated and reported in the literature [1]–[3]. However, these MMIC's were examined only on test fixtures or chip carriers. Unfortunately, they needed a certain external matching network or stub tuners in order to operate properly at the target frequencies. Since those external elements occupied a much wider area than the MMIC's themselves, size reduction of the oscillators was not achieved.

The key objectives of this study are 1) a full MMIC module configuration without external elements such as a dielectric puck resonator, I/O matching network, or interstage trimming board, 2) a package with all the needed chips mounted closely side by side, and 3) accurate design of each chip for proper operation without any trimming.

In this paper, we present a systematic development of MMIC's intended for very small oscillators, the resultant configuration of the MMIC's, and the measured performance of the developed oscillator module.

First, the development target and design concept for the system are described. Phase locking techniques to stabilize the frequency of the oscillator are discussed, and the phase-locked oscillator configuration suitable for the MMIC implementation is shown in comparison with the conventional hybrid MIC approach.

Next, practical MMIC chips are installed in the phase-locked oscillator module. Some of the key prototype MMIC's were previously reported by the authors [4]. They are altered and rearranged for this compact module. Associate circuits to complete the module are also developed.

Then, the design and performance of the package developed for the oscillator module are described. A specific package structure is introduced for low-loss, high-isolation characteristics. Compact alignment of the chips into the package and mechanical reliability are also mentioned.

Finally, the measured performance of the overall module is shown. Phase-locking characteristics are successfully confirmed at the target frequencies in the *Ku*-band.

II. System Design

In most microwave communication systems, local oscillators are required to have high frequency stability—on the order of 10^{-6} to 10^{-7}. This high stability cannot be obtained merely with dielectric resonators. In conventional oscillators with hybrid MIC configurations [5], this frequency stability was obtained by using both high-Q dielectric resonators and phase-locking techniques employing microwave sampling phase detectors. Unfortunately, this approach is inappropriate for GaAs monolithic circuitry because 1) high-Q resonators are difficult to integrate in the monolithic chip; 2) the step recovery diodes for the sampling phase detectors cannot be fabricated using present GaAs MMIC processes; and 3) sampling phase detectors dissipate several hundred mW in driving power.

The key features of the design concept for the MMIC oscillator system are given in Table I, as compared to conventional MIC oscillator systems. The MMIC oscillator system employs the direct division phase-locked oscillator (PLO) scheme as shown in Fig. 1. In this scheme, the voltage-controlled oscillator (VCO) is composed of only

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TABLE I
DESIGN CONCEPT OF THE MMIC PLO COMPARED TO HYBRID MIC PLO

	Present MMIC PLO	Conventional HMIC PLO
Resonator	Microstrip + Varactor	Dielectric puck
Resonance Q factor	≈ 10	≈ 10^3
Tuning range	≈ GHz	≈ MHz
Phase lock means	Frequency divider + Phase/frequency comparator	Sampling phase detector with step-recovery diode
Phase noise	Suppressed by phase locking to reference oscillator	Mainly dominated by Q factor of resonator
Loop response	100kHz ~ 1MHz	100Hz ~ 1kHz

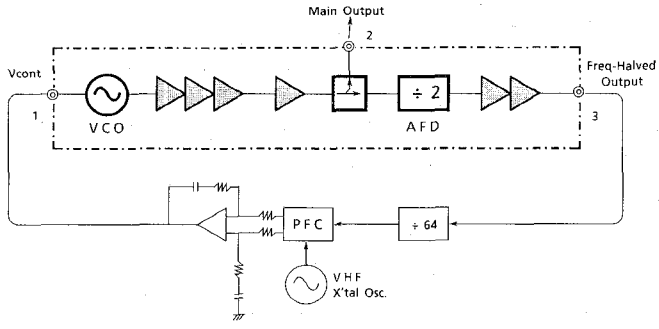

Fig. 1. *Ku*-band PLO block diagram.

monolithic elements without external resonators. A varactor diode is integrated and coupled tightly to the FET circuit, so that a wide tuning range, on the order of GHz, is obtained. On the other hand, the VCO also has greater frequency fluctuation than that of high-Q oscillators. This results in higher phase noise. In order to suppress the phase noise, the VCO is tightly locked to the very clean crystal oscillator, and the loop response is made much faster than in conventional oscillators. A more detailed discussion of the loop design is given in [6].

The phase-locked loop consists of a frequency divider and a phase detector. The frequency divider is composed of analog and digital stages. A Miller-type analog frequency divider [2] is used for the higher frequency stage, and high-speed digital frequency dividers [7] are employed for the lower frequency stages. The phase detector is also composed of high-speed digital circuits [8].

The whole system is integrated in the PLO module except for the digital circuits, i.e., the digital frequency divider and the phase/frequency comparator (PFC). The digital circuits were developed with silicon bipolar super self-aligned technology (SST) [7], [8], and are used here to provide the PLO module's phase-locking function.

Two key points arise when attempting to embody this system design and develop a practical module. One is the fully monolithic integration of each constituent circuit. The other is multichip packaging of the MMIC's in a compact manner. The constituent MMIC's and the package are designed as described in the following two sections, considering these two points.

III. CIRCUIT CONFIGURATION

The circuit configuration of the module is shown in Fig. 2 along with its constituent chips:

a) voltage-controlled oscillator (VCO) chip,
b) three-stage buffer amplifier chip,
c) one-stage limiting amplifier chip,
d) power splitter chip,
e) analog frequency divider (AFD) chip,
f) two-stage feedback amplifier chip.

Tuned by the control voltage, the VCO generates a CW signal in the *Ku*-band. The signal is amplified and splits in two ways. One is to the output port arranged on a side of the module, and the other leads to the AFD. The AFD halves the frequency, so the *Ku*-band signal is converted into the 7 GHz band. For leveling this signal and output isolation, a two-stage amplifier follows the AFD. Features of these circuits are described below.

The VCO chip includes a 0.5 μm×300 μm gate MESFET, a 2 μm×75 μm finger Schottky barrier varactor diode, and their matching and biasing networks. A common-drain FET circuit [4], [6] was used to obtain a wide tuning range and low pulling figure. The varactor diode was coupled to the common-drain FET via a quarter-wavelength microstrip transformer. A resistor was connected to the microstrip impedance transformer. This resistor functions not only as a biasing circuit but also as a Q-damping element to intentionally increase the circuit loss at out-of-band frequencies. This prevents unwanted parasitic oscillations. The VCO chip measures 2.0 mm×2.4 mm.

The buffer amplifier employs a three-stage linear amplifier to obtain enough gain to saturate the one-stage amplifier which follows it. Therefore, the output amplitude versus frequency curve becomes flat even if the VCO exhibits amplitude ripple. With this limiting amplifier, the input level of the AFD is also kept constant for the sake of proper operation of the AFD. The buffer amplifier (1.4 mm×4.0 mm) and limiting amplifier (1.4 mm×2.0 mm) employ the same FET's as the VCO chip.

The AFD employed here is the Miller frequency divider. The prototype MMIC Miller frequency divider was already developed and reported by the authors [2]. To describe it briefly, it is a down-converter with a feedback loop consisting of a balanced mixer and a filtering amplifier. In this feedback loop, a two-stage feedback amplifier was employed to obtain enough gain to compensate for the mixer loss. In addition, an interdigitated quadrature coupler was employed to provide enough isolation to avoid self-oscillations. This basic configuration has been revised to suit the present PLO module. The layout pattern of the present AFD is intended for compact packaging, resulting in a chip smaller than the prototype. The present AFD chip measures 4.0 mm×6.0 mm. A two-stage amplifier is again used after the AFD. This chip is designed to put out

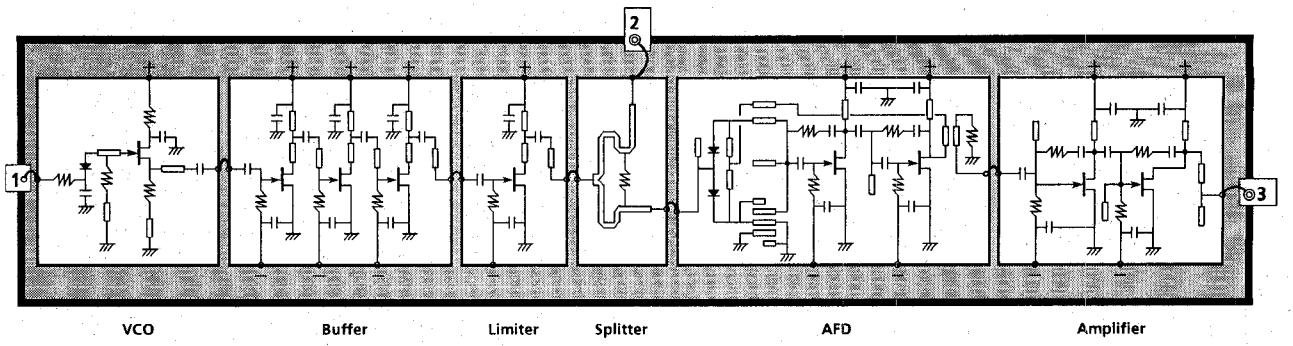

Fig. 2. Full MMIC module circuit diagram.

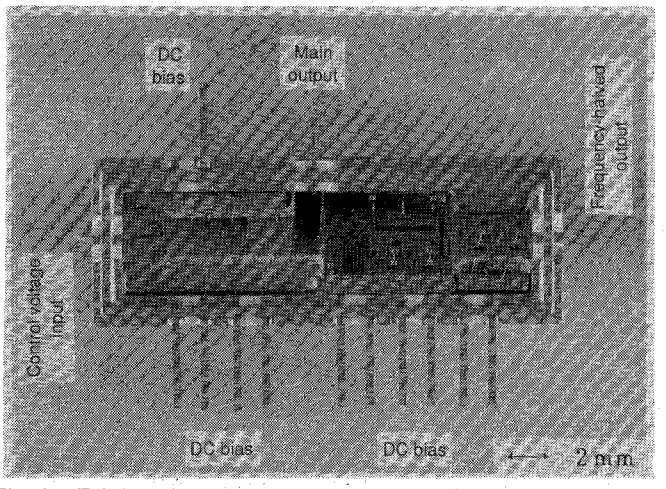

Fig. 3. Fabricated full MMIC module (before cover sealing). Six chips of MMIC are integrated in a 8 mm×23 mm flat metal package.

a signal level adequate for driving the digital divider in the system shown in Fig. 1.

All the above-mentioned monolithic chips fit the system diagram with respect to the frequency and the power level. In order to apply the chips in practical systems rather than on-wafer or test-fixture measurements, a high-performance package has been developed. Details of the package are described in the next section.

IV. Package

The high-performance package especially intended for the MMIC module is a flat type, equipped with three RF signal pads and 11 dc power pads, as shown in Fig. 3. The RF signal pads are assigned to the main output, the frequency-halved output, and the control voltage input. The dc power pads are assigned to the positive and negative bias supply for the MMIC chips. Though the control voltage input port does not handle microwave signal, it should be regarded not as a dc pad but as an RF pad. This is because 1) the VCO has high modulation susceptibility of 1 GHz/V, so that it should be well shielded against external noise, and 2) the VCO is to be kept in phase lock tightly enough to suppress quick phase fluctuations up to the MHz order.

The package design incorporates the following features. The first feature is assurance of high isolation between the RF terminals. In microwave IC packages, electromagnetic resonances would degrade the RF isolation characteristics and should not appear in the signal frequency range. There are two kinds of electromagnetic resonance in microwave packages. One is ring resonance by wave propagation guided dielectrically along the frame insulator of the package, and the other is cavity resonance like a metal-waveguide mode. In both kinds of resonance, the resonant frequency depends on the package material and structure. If the package frame is made of ceramic materials, the ring resonances may arise at GHz frequencies for this cavity size. Therefore, the present frame is made entirely of metal except for the terminal insulation. The terminal has a buried-ceramic structure in the frame as shown in Fig. 3. The base and the cap are also made of metal and the inside space is as narrow as possible to expel cavity resonance from the signal frequency band.

The next feature is low insertion loss for the RF terminals. The buried-ceramic terminal is looked upon as a short transmission line. This line behaves as a microstrip inside or outside of the package, and behaves as a shielded microstrip in the transition from inside to outside [9]. The insertion loss is mainly dominated by the reflection at this transition. In order to minimize the reflection, aspect parameters of the structure were optimized so that the characteristic impedance becomes 50 Ω in both the microstrip and the shielded microstrip. The structure optimization was carried out by means of spectral-domain electromagnetic field analysis [10].

The last feature is the mounting space for the fine alignment of the MMIC chips into the package. The chips were mounted side by side with Au–Sn solder on the metal base. The area required for the chip mounting is close to that of the chips. The rest of the space is occupied by biasing circuit elements such as the chip capacitors. Gaps between adjacent MMIC chips are kept to within 0.1 mm, so that the chips are cascaded by bonding wires with less stray inductance than 0.1 nH.

A performance test was carried out before mounting the MMIC chips. To estimate the terminal loss, the package was loaded with a ceramic substrate 50 Ω through line between two terminals. The terminal loss was obtained by half of the difference between total loss and line loss. Isolation between the terminals was measured with an empty package on the test fixture. The data obtained for insertion loss per terminal and the isolation between termi-

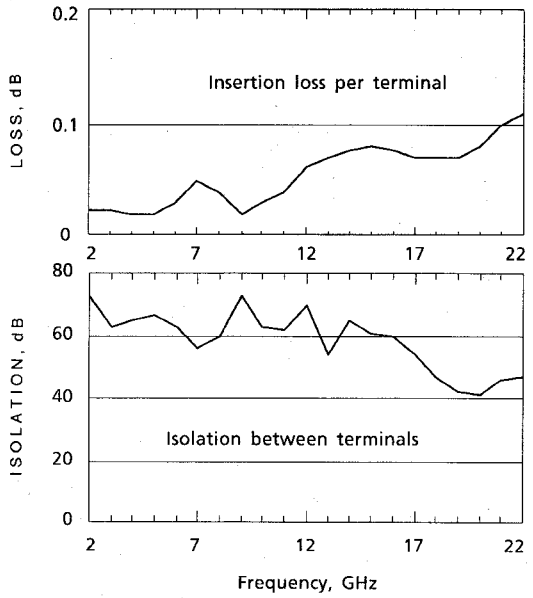

Fig. 4. Package terminal loss and isolation versus frequency.

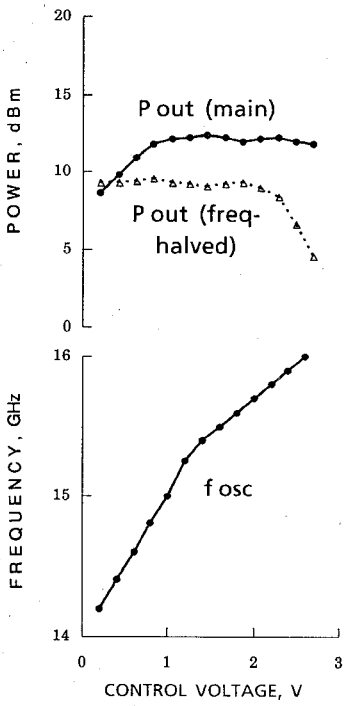

Fig. 5. Module tuning characteristics.

nals are depicted in Fig. 4. Neither serious dips nor peaks are found in the frequency responses up to 22 GHz.

Reliability tests based on the MIL-STD 883, thermal shock, helium leakage, and mechanical lead strength tests were also carried out. Since no failure mode was indicated in these tests, the present package is inferred to be applicable even to spaceborne equipment.

The features of the proposed MMIC package are 1) isolation over 40 dB with no resonance through 22 GHz, 2) insertion loss less than 0.1 dB per terminal through

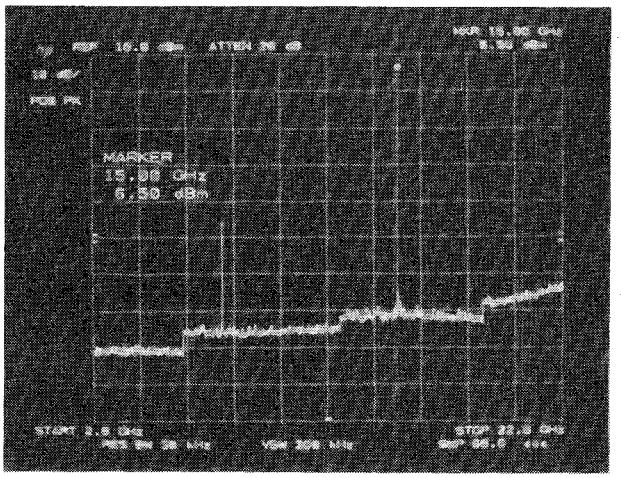

Fig. 6. Signal spectrum at main output port. H: 2 GHz/div; V: 10 dB/div; center: 12 GHz; resolution bandwidth: 30 kHz; video bandwidth: 300 kHz.

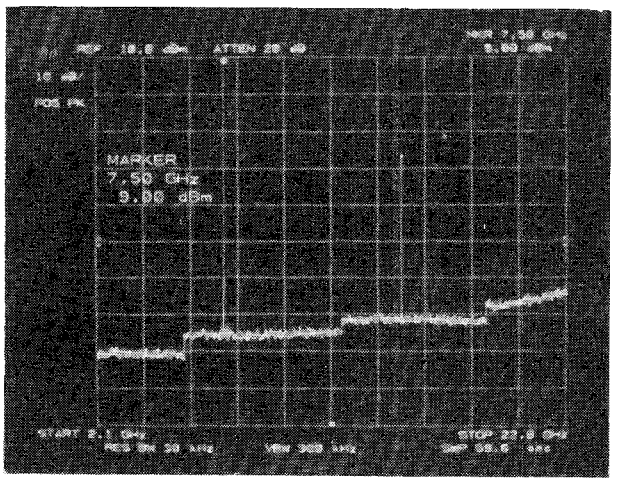

Fig. 7. Signal spectrum at frequency-halved output port. H: 2 GHz/div; V: 10 dB/div; center: 12 GHz; resolution bandwidth: 30 kHz; video bandwidth: 300 kHz.

20 GHz, 3) compact chip alignment and a packaging size of 8 mm×23 mm×3 mm, and 4) high mechanical/thermal reliability to the space application level.

V. Module Performance

Completed with all the chips mounted and covered with hermetic sealing, the module was tested in terms of oscillation and phase-locked characteristics. The measurements were carried out without any trimming or cut-and-try manipulation.

Measured tuning characteristics of the module are shown in Fig. 5. The oscillation frequency varies smoothly from 14.2 to 16.0 GHz. The output power versus control voltage is also plotted in this figure for the main output (solid line) and the frequency-halved output (dotted line). The amplitude characteristics have no ripples and exhibit good flatness in the middle 1 GHz of the tuning range.

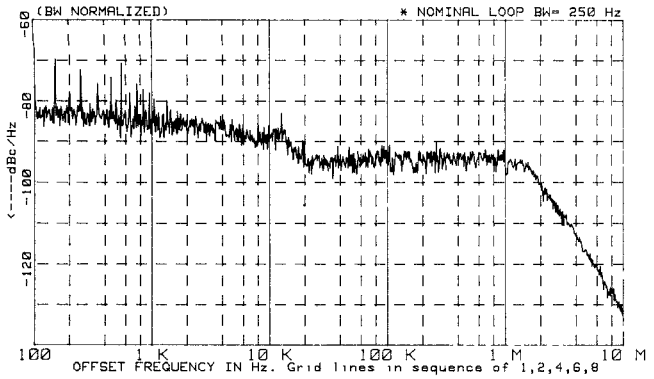

Fig. 8. PLO output SSB phase noise (f_{osc} = 15.0 GHz).

TABLE II
FULL MMIC MODULE PERFORMANCE

Characteristic	Value	Unit
Center frequency	15	GHz
Tuning range	1.7	GHz
Main output power	>8	dBm
Frequency-halved output power	>5	dBm
Phase noise at 100Hz - 10MHz offset	< -80	dBc/Hz
DC power dissipation	680	mW
Operational ambient temperature range	-10 ~ +40	°C
Dimensions	8×23×3	mm
Weight	7	g

Signal spectra observed at the main output port and the frequency-halved output port are shown in Figs. 6 and 7. The desired signals are indicated by the markers at 15.00 GHz or 7.50 GHz in the graphs. No parasitic oscillation can be found in the frequency range of 2–22 GHz. The second peak at 7.5 GHz in Fig. 6 is caused by the leakage of the frequency-halved signal from the AFD through the power splitter. This subharmonic D/U ratio is more than 40 dB. If a buffer amplifier were used before the AFD, the $1/2$ f signal leakage at port 2 might be improved. Conversely, the 15 GHz signal leaks to the frequency-halved output port, and is observed as the second harmonic in Fig. 7. This measures 26 dB below the fundamental signal.

A phase-locked loop was assembled and the output SSB phase noise was measured at 15.0 GHz. A graph of the results in Fig. 8 shows −80 dBc/Hz or less for 100 Hz–10 MHz off from the carrier. The fine spurious peaks observed in the 100 Hz–1 kHz range are due to the residual 50 Hz ripple in the ac/dc power supply of the measurement system. Phase-locking tests were done not only at room temperature but also at −10°C and +40°C. Phase locking did not fail at the high or the low temperature.

The confirmed characteristics of the PLO module are summarized in Table II. These values are suitable for most communication systems in the *Ku*-band.

VI. CONCLUSIONS

A *Ku*-band PLO module with a full MMIC configuration has been developed, incorporating a voltage-controlled oscillator, an analog frequency divider, interstage amplifiers, and some associate circuits. All the constituent MMIC's operate properly at the target frequencies without any trimming or external matching stubs. The oscillator is tuned more than 1 GHz with an almost constant output amplitude. The frequency-halved output is also obtained over the entire tuning range. Parasitic oscillation is not found at any frequency up to 22 GHz.

A phase-locking test was also carried out. It showed that the module performs well as a phase-locked oscillator with good spectral purity. In spite of the very low Q factor of monolithic circuitry, oscillator phase noise of less than −80 dBc/Hz was exhibited, due to phase locking with a quartz crystal reference oscillator. Since the proposed MMIC PLO module is more compact and has a much wider tuning range than conventional hybrid MIC PLO's, it is a candidate for very small *Ku*-band microwave synthesizers.

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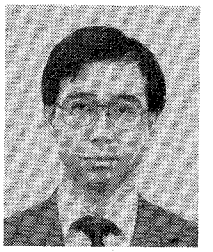

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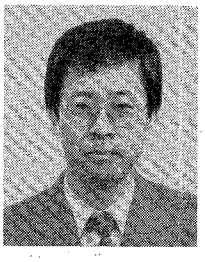

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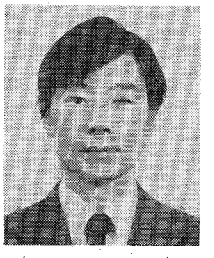
Mr. Kato is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



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